

REMARKS/ARGUMENTS

Applicant responds herein to the Office Action dated January 19, 2006. A Petition for Extension of Time (one month) and the fee therefor are enclosed.

Claims 1-9 are amended. The amendments to these claims are for clarification purposes only, curing errors which may have been caused by translation, the amendments are not intended to limit the scope of these claims in any way. Furthermore, the amendments are merely explicitly stating what was already implicit in the claims.

Claims 4-9 are rejected under 35 U.S.C. §112 as being indefinite. These claims are amended, in light of the remarks in the Office Action, to more clearly define the invention. Reconsideration of the rejection of claims 4-9 under 35 U.S.C. §112 is respectfully requested.

Claims 1, 4 and 6-9 are rejected under 35 U.S.C. §103 as being unpatentable over Applicant's Admitted Prior Art ("APA") in view of U.S. Patent 6,043,694 to Dortu ("Dortu"). Reconsideration of the application in light of the amendments and remarks below is respectfully requested.

In order to establish a prima facie case of obviousness: 1) the prior art in combination must show all of the claimed limitations and 2) there must be a suggestion or motivation in the prior art to combine the prior art as suggested in the Office Action, See, e.g., M.P.E.P. §706.02(j). Both elements are missing here.

As a general comment, APA does not disclose any means for outputting the comparison result as the phase advance/delay signal to the external, output unit. That alone serves to distinguish over the prior art.

Further, among the limitations of independent claims 1, 4, 5 and 8 which are neither shown nor suggested even in a combination of APA and Dortu are:

a phase advance/delay signal generation unit, the phase advance/delay signal generating unit effective to selectively compare the internal clock signal and either one of the external clock signal and the output signal of the data output circuit to produce a phase advance/delay signal indicating whether the phase of the output signal of the data output circuit advances or delays with respect to the phase of the external clock signal.

The Office Action points to both Figure 1, with specific reference to designators 24, 28 and 30, and column 5, lines 5-8 and 23-34 of Dortu as showing the above referenced limitation. Figure 1 relates to a prior art embodiment in Dortu and column 5 discusses a preferred embodiment of the Dortu invention. As an initial matter therefore, the two alleged teachings in these sections do not relate to a single structure.

In Figure 1 of Dortu, phase comparator 28 compares an output from either delay line 22 or driver 24 with the output from receiver 20. Contrary to the assertion made in the Office Action, there is no teaching of a phase advance/delay signal generating unit effective to selectively compare the internal clock signal and the output signal of the data output circuit – as is claimed. Though the Office Action states that Dortu uses the output signal from the “driven circuit”, Applicant respectfully asserts that phase comparator 28 of Dortu looks at the output of driver 24 and not a “driven circuit” and certainly not a data output circuit – as is claimed.

Similarly, column 5 of Dortu discusses the operation of Fig. 3 which shows phase comparator 58 comparing the output from receiver 50 with the output of driver 54 (through receiver 56). Again, contrary to the assertion made in the Office Action, there is no teaching of a phase advance/delay signal generating unit effective to selectively compare the internal clock signal and the output signal of the data output circuit – as is claimed. Though the Office Action states that Dortu uses the output signal from the “driven circuit”, Applicant respectfully asserts that phase comparator 58 of Dortu looks at the output of driver 24 and not a “driven circuit” and certainly not a data output circuit – as is claimed.

Furthermore, independent claims 1, 4, 5 and 8 also state that the phase advance/delay signal generating unit is effective to selectively compare the internal clock signal and either one of the external clock signal and the output signal of the data output circuit. No where even in a combination of APA and Dortu is there a teaching enabling such a selective comparison as claimed.

Therefore, it is asserted that claims 1, 4, 5 and 8 are patentable over even a combination of APA and Dortu. Claims 2, 3, 6, 7 and 9 include the above referenced limitations of claims 1 and 8 and include additional recitations which, when combined with the limitations of claims 1

and 8, are also neither disclosed nor suggested in the art of record. It is asserted that these claims are patentable as well.

Additionally, there is no motivation cited in the Office Action for combining APA and Dortu. The Office Action simply states it would have been obvious to combine the two pieces of prior art and indicates that such a combination would cover a "deficiency" of APA. However, no motivation is cited or is shown in the prior art for actually making this modification – as is required for a *prima facie* case of obviousness.

Therefore, reconsideration of the rejection of claims 1-9 under 35 U.S.C. §103 is respectfully requested in light of the remarks above.

Applicant notes with appreciation that claims 2, 3 and 5 were indicated as being allowance if rewritten in independent form. However, Applicant chooses to defer a rewriting of these claims until a final resolution of the above matters.

Accordingly, the Examiner is respectfully requested to reconsider the application, allow the claims as amended and pass this case to issue.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 21, 2006

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April 21, 2006

Date of Signature

Respectfully submitted,

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